REMARKS

Applicants thanks Examiner for their detailed review of the application. Applicant amended claims 31, 40, 45, 48-51, and 54-59.

Claim objections

The Office Action objected to claims 31 due to informalities. Claim 31 has been amended to correct the antecedent basis problem changing the reference in line 5 from "the second SMBase" to "the second SMBase address." Consequently, applicant respectfully submits that proper antecedent basis has been provided in claim 31.

Claim Rejections – 35 USC 102

The Office Action rejects applicants claim 54-59 and 61 under 35 U.S.C 102(b) as being anticipated by Nguyen et al. (US 2002/0099893), herein referred to as Nguyen. Applicant's claim 54 includes the elements, "**a first processor … to execute the SMI code beginning at the first memory address** to handle an SMI for the first processor…and **a second processor to execute the SMI code** beginning at the first memory address to handle the SMI for the second processor **in response to the SMI being software generated**," (emphasis added). Note, that both the first processor and the second processor execute the SMI code beginning at the first memory address to handle the SMI in response to the SMI being software generated in applicant's claim 54.

In contrast, Nguyen explicitly designates only one processor to execute SMI code, i.e. processor 12c in paragraph 0018, not both the first and second processor in response to the SMI being software generated. Processor 12b, which Nguyen discloses as the processor that issued the instruction to cause the software SMI, only saves its signature to SMRAM space, and does not execute SMI code; let alone SMI code beginning at the same memory address. Nguyen teaches that processor 12c, through execution of **its SMI handler**, handles the SMI for processor 12b, since it is designated as the single processor to handle SMIs. Note that not only does Nguyen teach only a

single processor executing SMI code to handle SMIs for all processors with parameters passed to it from other processor's SMRAM space, but implies each processor is associated with **its own** SMI handler. This can be seen through Nguyen's use of the language: processor 12 through execution of **its SMI handler** Instead, applicant's claim 54 includes both processors execute SMI code beginning at the same memory address, i.e. the first address, not a single default processor to execute SMI code to handle SMIs for all processors as in Nguyen.

Next, The Office Action rejects claims 45 and 47-49 under 102(a) as being anticipated by Dale (GB 2382180A).

Examiner rejects claims 45, and 47-49 under 102(a) as being anticipated by Dale (GB 2382180A). Applicant's claim 45 includes the elements, "the first processor is to execute the code beginning a the first memory address…the second processor is to execute the code beginning at the first memory address," (redacted). Dale only discloses that GPIO unit of the MMI sub-system generates an interrupt to wake MMI processor 322 (see page 19 lines 30-31). In addition, Dale only suggests on page 19 at lines 1-4, that the wake up process is initiated and the GSM processor performs the task which it was woken up for. However, nowhere does Dale suggest both processors executing code beginning at a same memory location, but rather only access the same memory element, i.e. shared memory.

Furthermore, applicant's claim 45 includes the element, "the first processor …to receive the first SMI…and is to **generate a wake-up signal after receiving the first SMI**…a second processor…to receive the first SMI, to be woken up in response to receiving the wake-up signal," (redacted). Here, the office action equates applicant's first SMI to Dale's Radio ON signal, applicant's first processor to Dale's GSM processor and applicant's second processor to Dale's MMI processor. However, Dale's expressly states that the GSM processor sets the Radio ON signal, which is provided to the MMI sub-system, which in turn generates an interrupt to wake-up

the MMI processor. As can be seen, Dale's GSM processor does not generate a wake-up signal after receiving the first SMI, but rather only generates the Radio ON signal after timer expiration. The MMI sub-system then generates the interrupt that wakes up the MMI processor, not the GSM processor. As a result, both of Dale's processors do not receive the Radio ON signal, i.e. what the Office Action equates to applicant's first SMI. In addition, the GSM processor, which is analogized to applicant's first processor, does not generate a wake-up signal after "receiving" the RADIO ON signal which wakes up the second processor, i.e. the MMI processor.

Claim Rejections – 35 USC 102

The Office action rejects claim 40 and 41 under U.S.C. 103 as being unpatentable over Dale in view of Nalawadi (US 2003.0009654 A1). However, claim 40 includes the limitation of "a first logical processor…to handle the first SMI and generate a wake-up signal **after the first SMI**, as discussed above in reference to claim 45. Furthermore, Dale GSM sub-system only generates the RADIO-ON signal, which is described only as a voltage level on page 18, not a wake-up signal that "references a first memory address of a default SMI handler," as in applicant's claim 40. Also noted above, is that the GSM processor fetches and executes instructions from memory 350, but Dales does not disclose that the instructions are part of a default SMI handler and does not suggest that the location of those instructions is referenced in the RADIO-ON signal or interrupt generated by the GPIO. Additionally, Nalawadi is used in combination for logical processors; however, Nalawadi does not disclose the wake-up signal being generated by the first processor after receiving the first SMI or that a wake-up signal references a default SMI handler.

Consequently, applicant respectfully requests that independent claim 40, 45, and 54, as well as their dependent claims are now in condition for allowance for the reasons stated above. Furthermore, applicant notes that independent claims 1, 12, 26, and 32, which were previously designated as allowable in The Office Action, have not been amended, and therefore, applicant

respectfully submits that they are still in condition for allowance. Applicant again thanks Examiner for their detailed review of the application.

If there are any additional charges, please charge Deposit Account No. 50-0221. If a telephone interview would in any way expedite the prosecution of the present application, the Examiner is invited to contact David P. McAbee at (503) 712-4988.

Respectfully submitted,
Intel Corporation

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